CMOS single-chip 8-bit MCU with 10-bit A/D converter and LCD driver

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 12Kbytes Flash Code Memory
  - 256bytes SRAM(IRAM 256bytes)
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 8 MHz HFIRC Oscillator (±1.0%, T_A= -10 ~ +55°C, User trim)
  - Internal 32 kHz LFIRC Oscillator (±10.0%, T_A= -10 ~ +55°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 10-bit Analog to Digital Converter (8 inputs)
  - LCD Driver (26 Segments x 8 Commons)
  - 16-bit CRC/Checksum Generator
  - Built-in Transistor for IR LED Drive
- **I/O and Packages**
  - 6 I/O, 39 Shared I/O with LCD signal
  - 50Pellet, 48LQFP
  - Pb-free package
- **Operating Conditions**
  - 1.8V to 3.6V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Home appliance, Industrial Control

A96R725

Data Sheet

V 1.0

7 September, 2018

Revision history

Version	Date	Revision list
1.0	2018.09.07	Published this book.

Version 1.0

Published by FAE team

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1 Overview

1.1 Description

The A96R725 is advanced CMOS 8-bit microcontroller with 12Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 12Kbytes of FLASH, 256bytes of IRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, carrier generation, watch timer, 10-bit A/D converter, LCD driver, 16-bit CRC/Checksum Generator, Built-in Transistor for I.R LED Drive, Built-in Transistor for LCD Back Light Drive, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The A96R725 also supports power down modes to reduce power consumption.

Device Name	FLASH	IRAM	ADC	I/O PORT	Package
A96R725	12Kbytes	256bytes	8inputs	45	50-Pellet
A96R725CL			8inputs	45	48LQFP-0707

Table 1.1 Ordering Information of A96R725

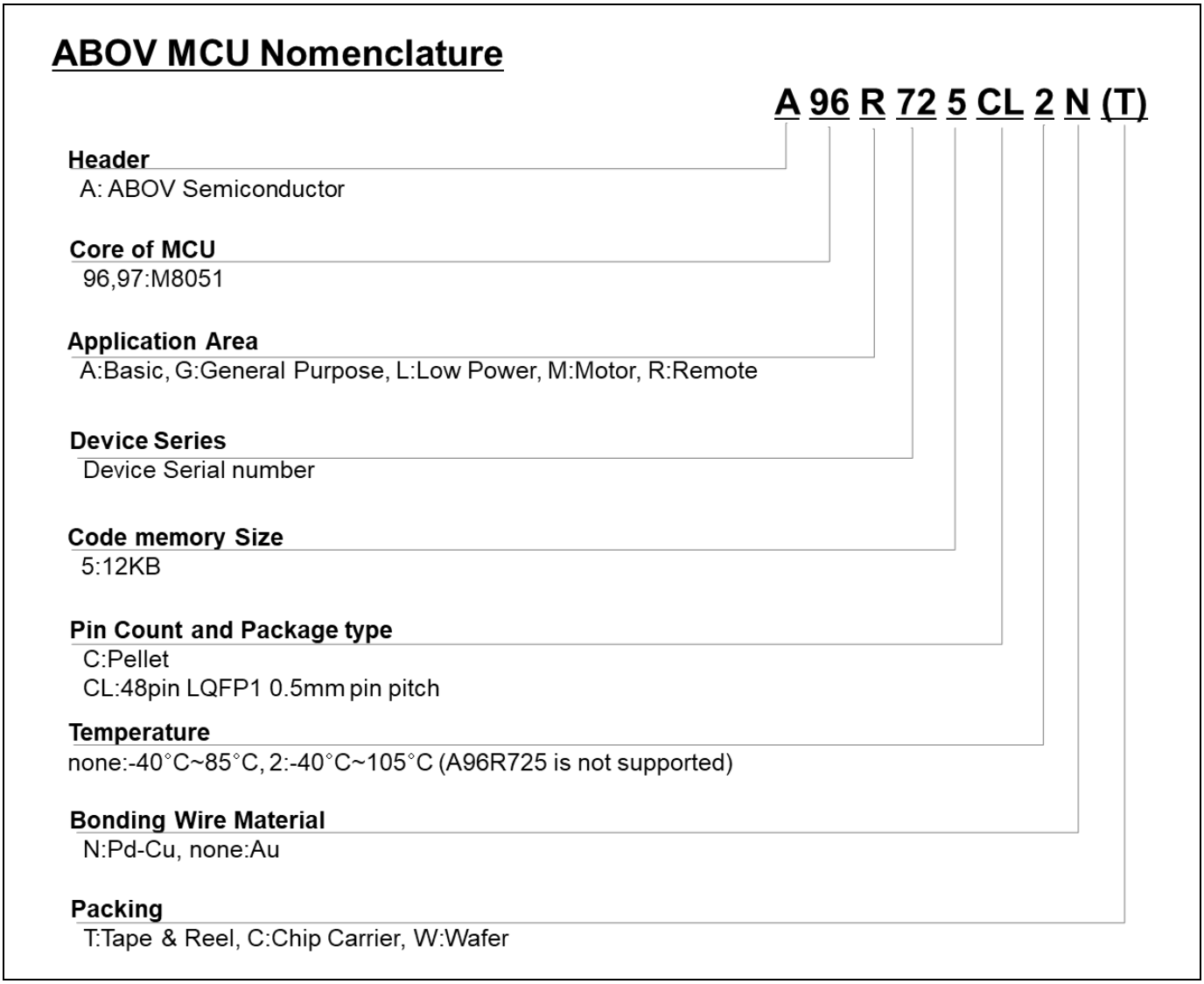


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 12Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 times(Sector 0~375)
    100,000 times(Sector 376~383)
  - Retention : 10 years
- **256bytes SRAM**
  - Excluding 32bytes for LCD display
- **General Purpose I/O (GPIO)**
  - Normal I/O : 6 Ports
    (P4[5:0])
  - LCD shared I/O : 39 Ports
    (P0[7:0], P1[7:0], P2[7:0], P3[7:0], P5[6:0])
- **Basic Interval Timer (BIT)**
  - 8-bit× 1-ch
- **Watch Dog Timer (WDT)**
  - 8-bit× 1-ch
  - 5kHz internal RC oscillator
- **Timer/Counter**
  - 8-bit× 2-ch(T0/T1), 16-bit× 2-ch (T2/T3)
  - 16-bit Interval Timer × 1ch
- **Carrier Generation**
  - Carrier generation (by T1), T3 Clock source
- **Programmable Pulse Generation**
  - Pulse generation (by T2/T3)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
- **10-bit A/D Converter**
  - 8 Input channels
- **LCD Driver**
  - 26 Segments and 8 Common
  - 1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty selectable
  - Voltage booster and 10-step contrast control
  - Internal/External resistor bias
- **16-Bit CRC/Checksum Generator**
  - Auto and User CRC/Checksum mode
- **Built-in Transistor for I.R LED Drive**
  - IOL = 630mA at 3V and VOL = 1.0V
- **Built-in Transistor for LCD Back Light Drive**
  - 2Pins, IOL = 10/20/30[mA] at 3V and VOL = 1.0V
- **Inverter Amplifier**
  - 3-ch high-gain inverter amplifiers
- **Power On Reset**
  - Reset release level (1.2V)
- **Low Voltage Reset**
  - 4 level detect (1.62V, 2.0V, 2.4V, 2.68V)
- **Low Voltage Indicator**
  - 3 level detect (2.0V, 2.4V, 2.68V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0 ~ EINT7, EINT12, EINT13) (10)
  - Timer0/1/2/3 (4), Interval Timer (1)
  - WDT (1), BIT (1), WT (1)
  - ADC (1), , LVI (1)
- **Internal RC Oscillator**
  - HFIRC frequency:
    8MHz ±1.0% (T_A= -10 ~ +55°C, User trim)
  - LFIRC frequency:
    32kHz ±10.0% (T_A= -10 ~ +55°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 3.6V (@ 32 ~ 38kHz with SX-tal)
  - 2.0V ~ 3.6V (@ 0.4 ~ 4.2MHz with X-tal, Crystal)
  - 1.8V ~ 3.6V (@ 0.4 ~ 4.2MHz with X-tal, Ceramic)
  - 2.4V ~ 3.6V (@ 0.4 ~ 8.0MHz with X-tal)
  - 3.0V ~ 3.6V (@ 0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 3.6V (@ 0.5MHz ~ 8.0MHz with HFIRC)
  - 1.8V ~ 3.6V (@ 4.0kHz ~ 32.0kHz with LFIRC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 167ns (@12MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 50-Pin Pellet
  - 48-Pin LQFP-0707
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of A96R725 is Mentor 8051. And, device ROM size is smaller than 12Kbytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on all Microsoft-Windows operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site(http://www.abov.co.kr).

Connection:

- DSCL (A96R725 P20 port)
- DSDA (A96R725 P17 port)

OCD connector diagram: Connect OCD with user system

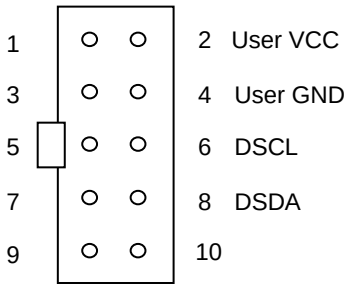


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

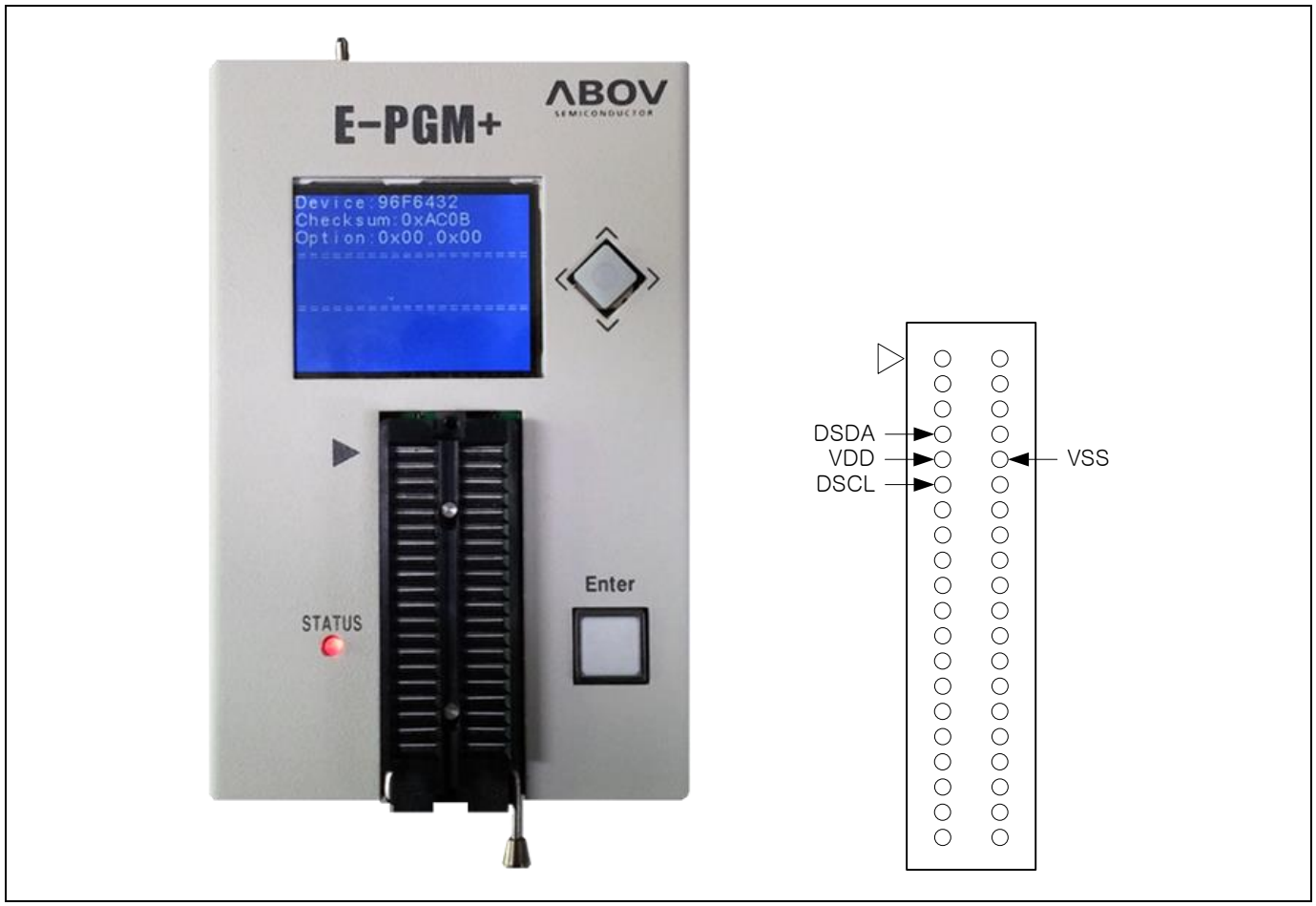


Figure 1.3 E-PGM+(Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of A96R725 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P20	I	Serial clock pin. Input only pin.
DSDA	P17	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

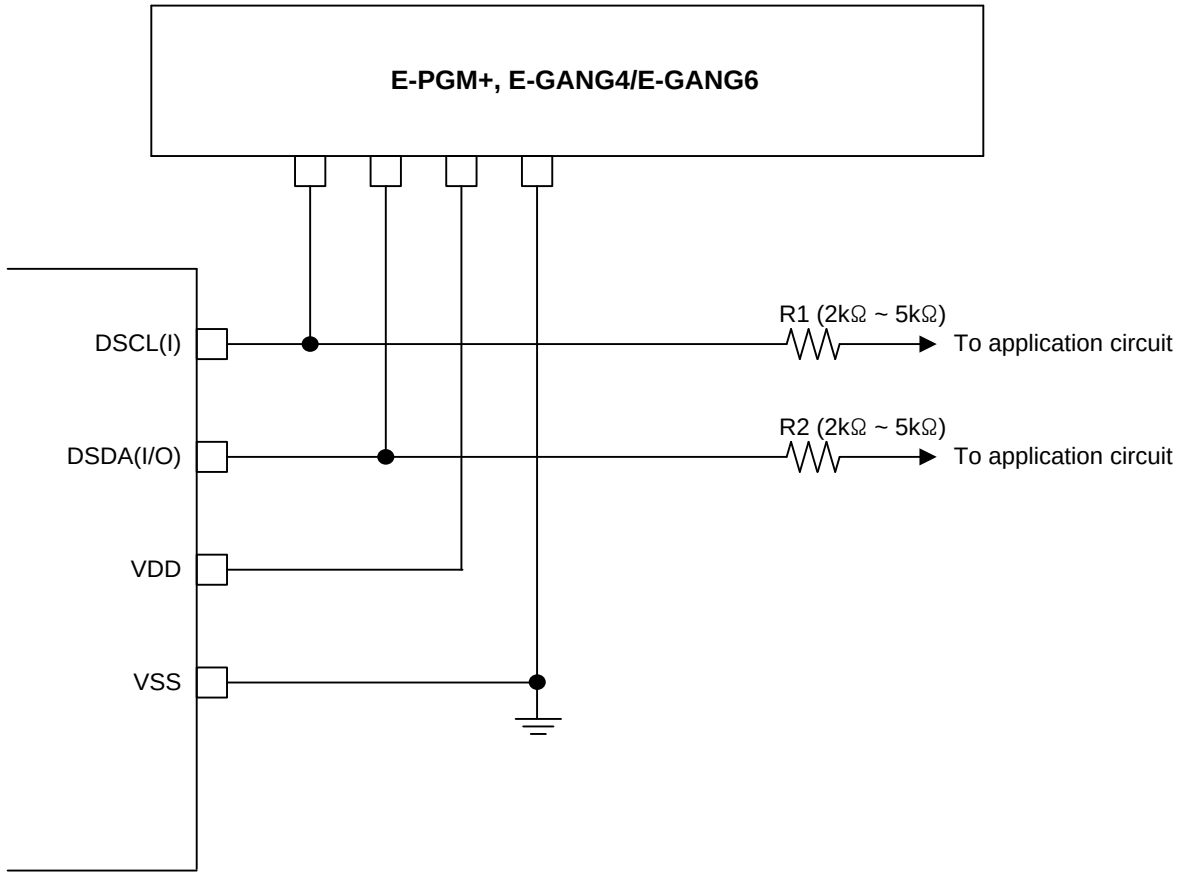
Table 1.2 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The A96R725 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming. Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

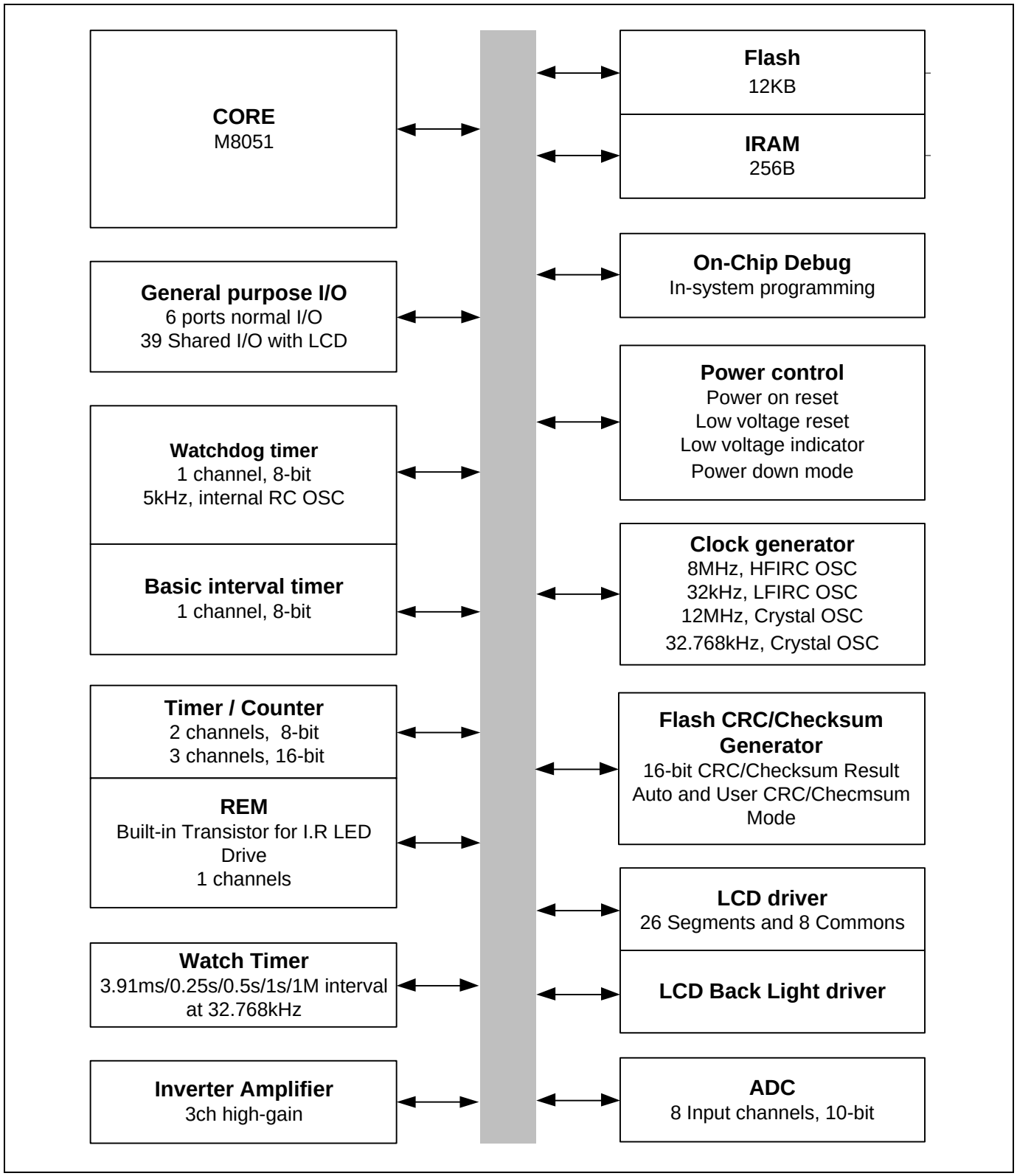
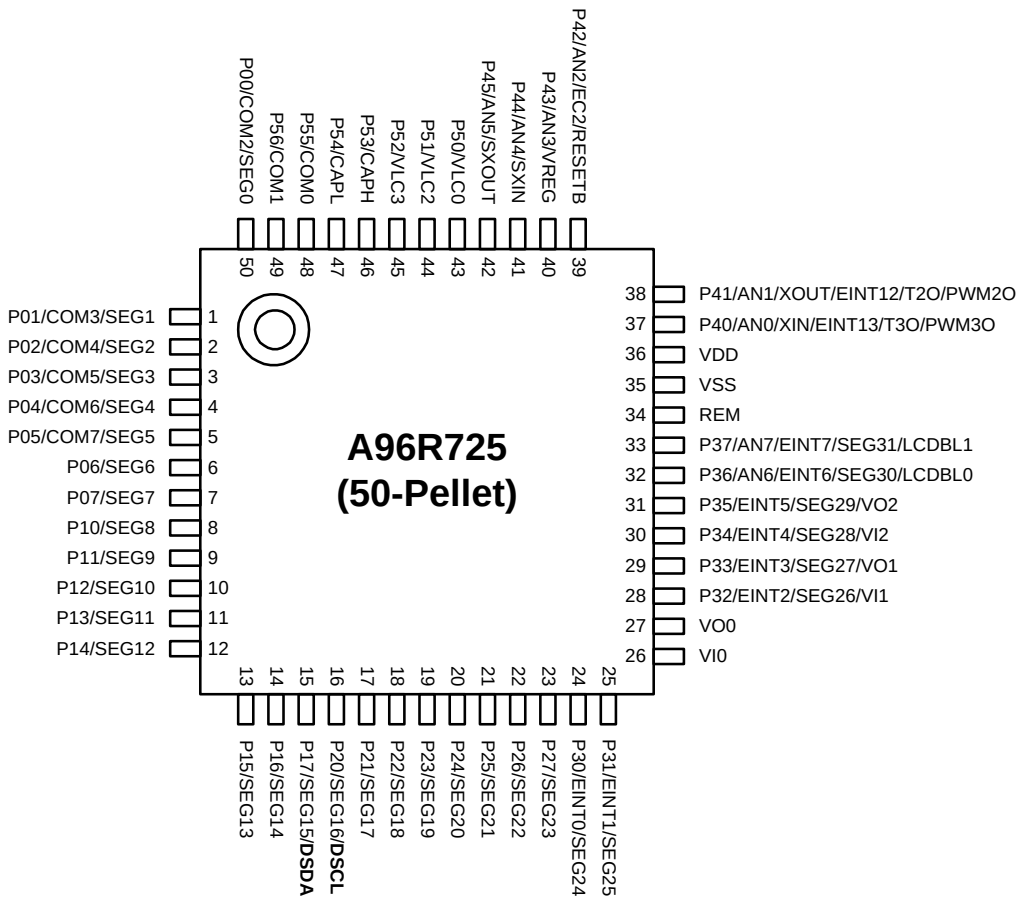


Figure 2.1 Block diagram of A96R725

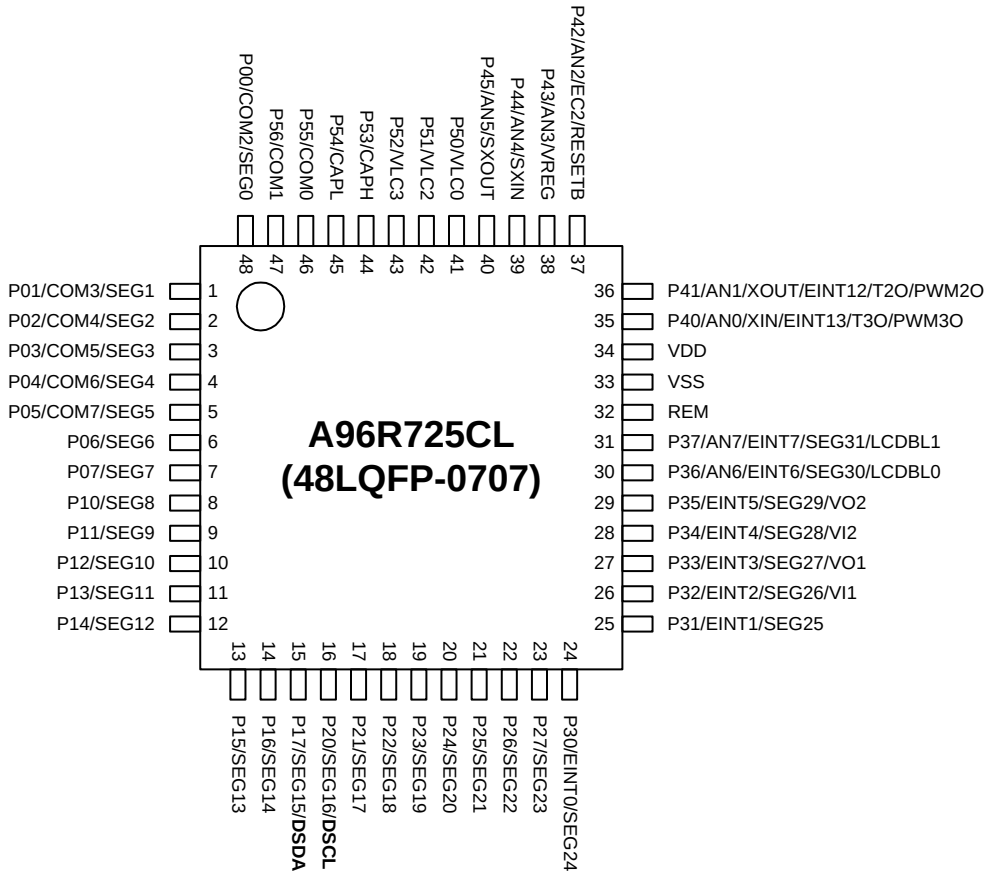
3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P20 and P17 pin as DSCL, DSDA.

Figure 3.1 A96R725 50 Pellet Pin Assignment

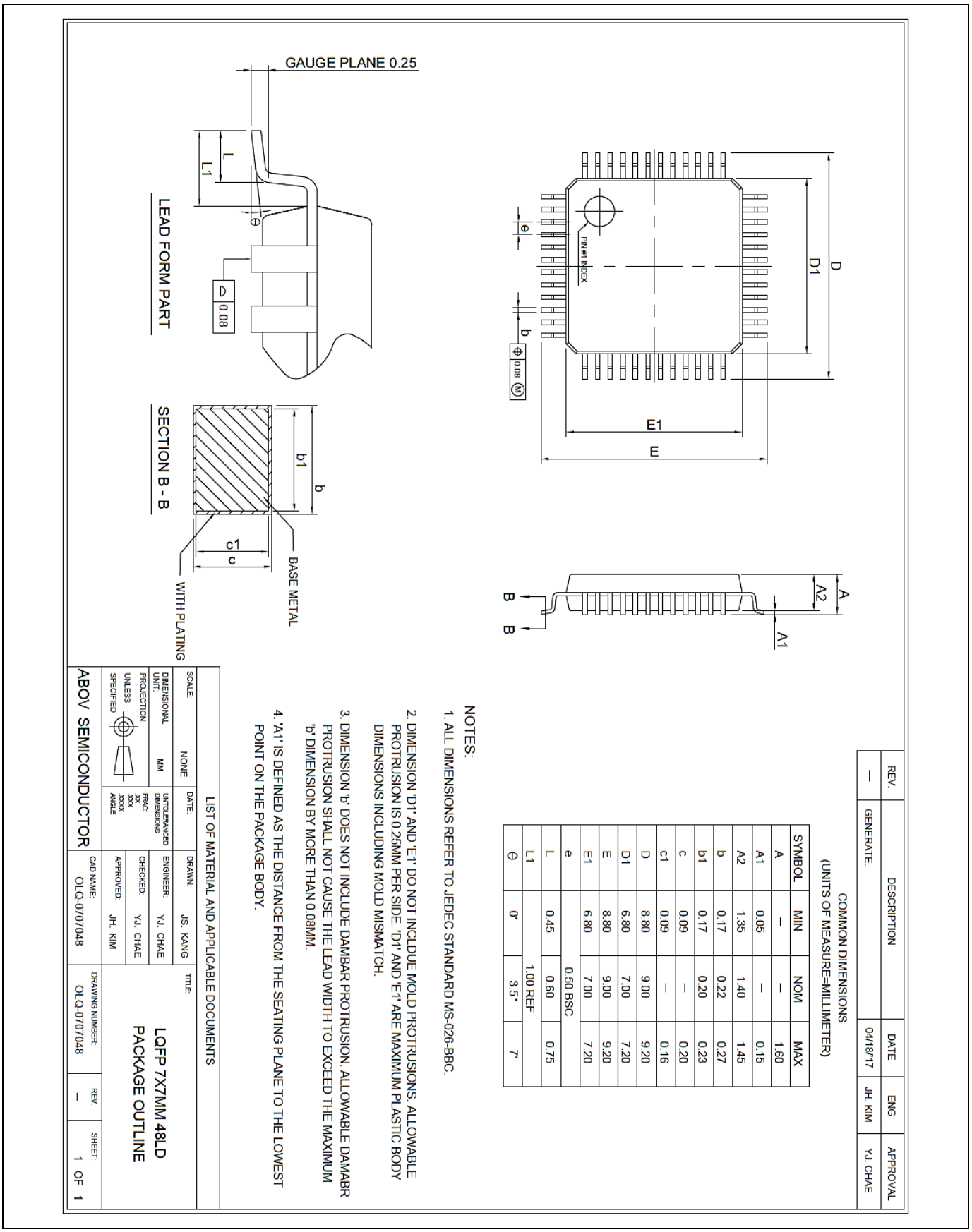


NOTE)

1. On On-Chip Debugging, ISP uses P20 and P17 pin as DSCL, DSDA.

Figure 3.2 A96R725CL 48 LQFP Pin Assignment

4 Package Diagram



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX .XX .XXX ANGLE	ENGINEER: YJ. CHAE	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
		APPROVED: JH. KIM	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	DRAWING NUMBER: OLQ-0707048	REV. —
			SHEET: 1 OF 1

Figure 4.1 48-Pin LQFP-0707 Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	COM2/SEG0
P01				COM3/SEG1
P02				COM4/SEG2
P03				COM5/SEG3
P04				COM6/SEG4
P05				COM7/SEG5
P06				SEG6
P07				SEG7
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as an input (P17: Schmitt-trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG8
P11				SEG9
P12				SEG10
P13				SEG11
P14				SEG12
P15				SEG13
P16				SEG14
P17				SEG15/DSDA
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input (P20: Schmitt-trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG16/DSCL
P21				SEG17
P22				SEG18
P23				SEG19
P24				SEG20
P25				SEG21
P26				SEG22
P27				SEG23
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT0/SEG24
P31				EINT1/SEG25
P32				EINT2/SEG26/VI1
P33				EINT3/SEG27/VO1
P34				ENIT4/SEG28/VI2
P35				EINT5/SEG29/VO2
P36				AN6/EINT6/SEG30/LCDBL0
P37				AN7/EINT7/SEG31/LCDBL1

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/XIN/EINT13/T3O /PWM3O
P41				AN1/XOUT/EINT12/T2O /PWM2O
P42				AN2/EC2/RESETB
P43				AN3/VREG
P44				AN4/SXIN
P45				AN5/SXOUT
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	VLC0
P51				VLC2
P52				VLC3
P53				CAPH
P54				CAPL
P55				COM0
P56				COM1
EINT0	I/O	External interrupt inputs	Input	P30/SEG24
EINT1				P31/SEG25
EINT2				P32/SEG26
EINT3				P33/SEG27
EINT4				P34/SEG28
EINT5				P35/SEG29
EINT6				P36/SEG30
EINT7				P37/SEG31
EINT12	I/O	External interrupt and Timer 12 capture input	Input	P41/AN1/XOUT/T2O/PWM2O
EINT13	I/O	External interrupt and Timer 13 capture input	Input	P40/AN0/XIN/T3O/PWM3O
T2O	I/O	Timer 2 interval output	Input	P41/AN1/XOUT/EINT12 /PWM2O
T3O	I/O	Timer 3 interval output	Input	P40/AN0/XIN/EINT13 /PWM3O
PWM2O	I/O	Timer 2 pulse output	Input	P41/AN1/XOUT/EINT12/T2O
PWM3O	I/O	Timer 3 pulse output	Input	P40/AN0/XIN/EINT13/T3O
EC2	I/O	Timer 3 event count input	Input	P42/AN2/RESETB
AN0	I/O	A/D converter analog input channels	Input	P40/XIN/EINT13/T3O /PWM3O
AN1				P41/XOUT/EINT12/T2O /PWM2O
AN2				P42/EC2/RESETB
AN3				P43/VREG
AN4				P44/SXIN
AN5				P45/SXOUT
AN6				P36/EINT6/SEG30/LCDBL0
AN7				P37/EINT7/SEG31/LCDBL1

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
REM	O	High current n-channel open-drain output for driving I.R. LED.	Output	–
LCDBL0	I/O	LCD back light drive pins	Input	P36/AN6/EINT6/SEG30
LCDBL1				P37/AN7/EINT7/SEG31
VI0	I	The input of a high gain inverter amplifiers	Input	–
VI1	I/O			P32/EINT2/SEG26
VI2				P34/ENIT4/SEG28
VO0	O	The output of a high gain inverter amplifiers	Output	–
VO1	I/O		Input	P33/EINT3/SEG27
VO2				P35/EINT5/SEG29
VLC0	I/O	LCD bias voltage pins	Input	P50
VLC2				P51
VLC3				P52
CAPH	I/O	Capacitor terminals for voltage booster	Input	P53
CAPL				P54
COM0	I/O	LCD common signal outputs	Input	P55
COM1				P56
COM2				P00/SEG0
COM3				P01/SEG1
COM4				P02/SEG2
COM5				P03/SEG3
COM6				P04/SEG4
COM7				P05/SEG5

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
SEG0	I/O	LCD segment signal outputs	Input	P00/COM2
SEG1				P01/COM3
SEG2				P02/COM4
SEG3				P03/COM5
SEG4				P04/COM6
SEG5				P05/COM7
SEG6				P06
SEG7				P07
SEG8				P10
SEG9				P11
SEG10				P12
SEG11				P13
SEG12				P14
SEG13				P15
SEG14				P16
SEG15				P17/DSDA
SEG16				P20/DSCL
SEG17				P21
SEG18				P22
SEG19				P23
SEG20				P24
SEG21				P25
SEG22				P26
SEG23				P27
SEG24				P30/EINT0
SEG25				P31/EINT1
SEG26				P32/EINT2
SEG27				P33/EINT3
SEG28				P34/EINT4
SEG29				P35/EINT5
SEG30				P36/EINT6
SEG31				P37/EINT7

Table 5.1 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P42/AN2/EC2
DSDA	I/O	On chip debugger data input/output	Input	P17/SEG15
DSCL	I/O	On chip debugger clock input	Input	P20/SEG16
XIN	I/O	Main oscillator pins	Input	P40/AN0/EINT13 /T3O/PWM3O
XOUT				P41/AN1/EINT12 /T2O/PWM2O
SXIN	I/O	Sub oscillator pins	Input	P44/AN4
SXOUT				P45/AN5
VREG	I/O	Regulator voltage output for sub clock 0.1uF capacitor needed	Input	P43/AN3
VDD, VSS	–	Power input pins	–	–

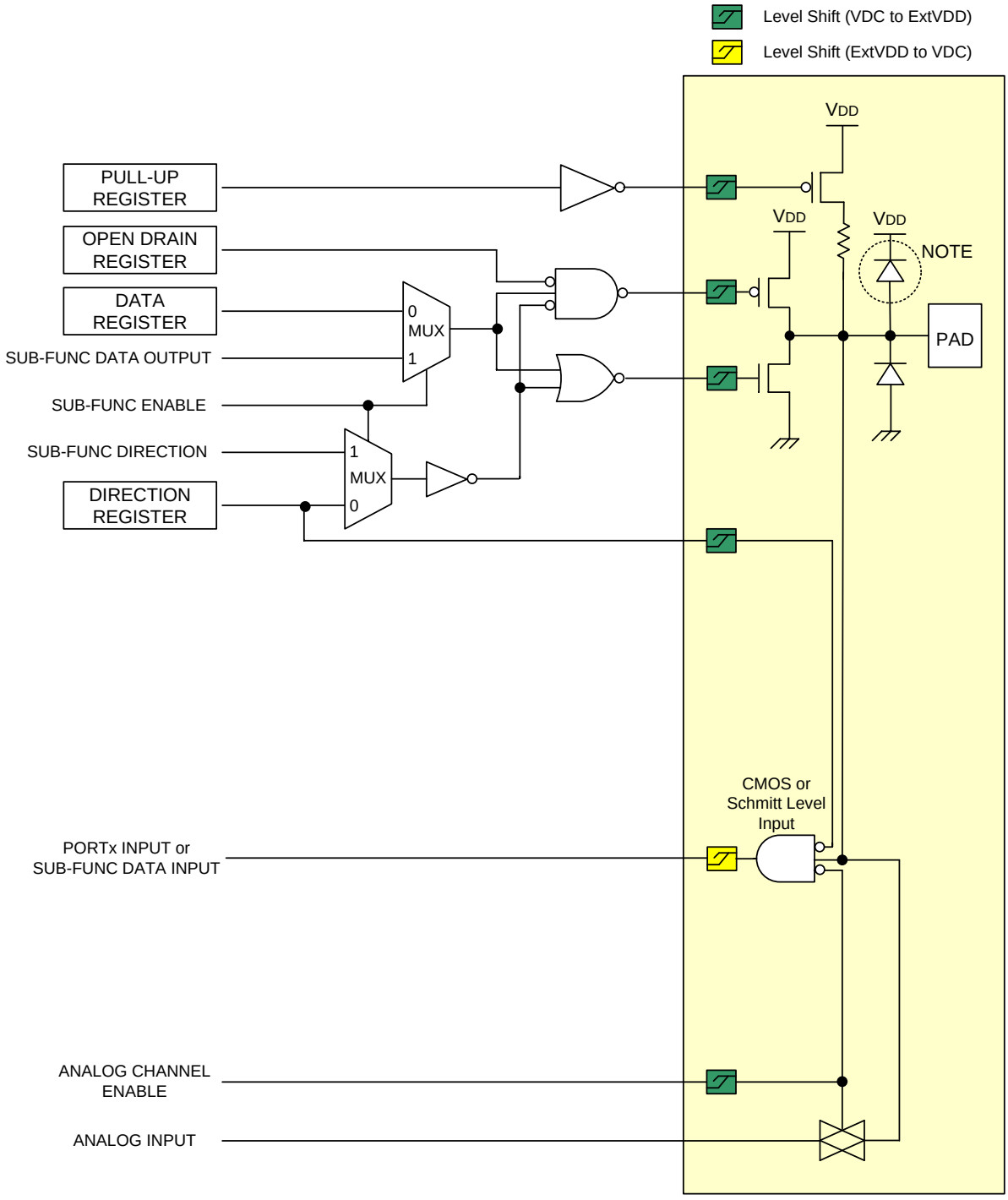
Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P42/RESETB pin is configured as one of P42 and RESETB pin by the “CONFIGURE OPTION”.
2. The P40/XIN and P41/XOUT pins are configured as a function pin by software control.
3. The P44/SXIN, P45/SXOUT, and P43/VREG pins are configured as a function pin by s/w control.
4. If the P17/SEG15/DSDA and P20/SEG16/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
5. The P17/SEG15/DSDA and P20/SEG16/DSCL pins are configured as inputs with internal pull-up resistors only during the reset or power-on reset.

6 Port Structures

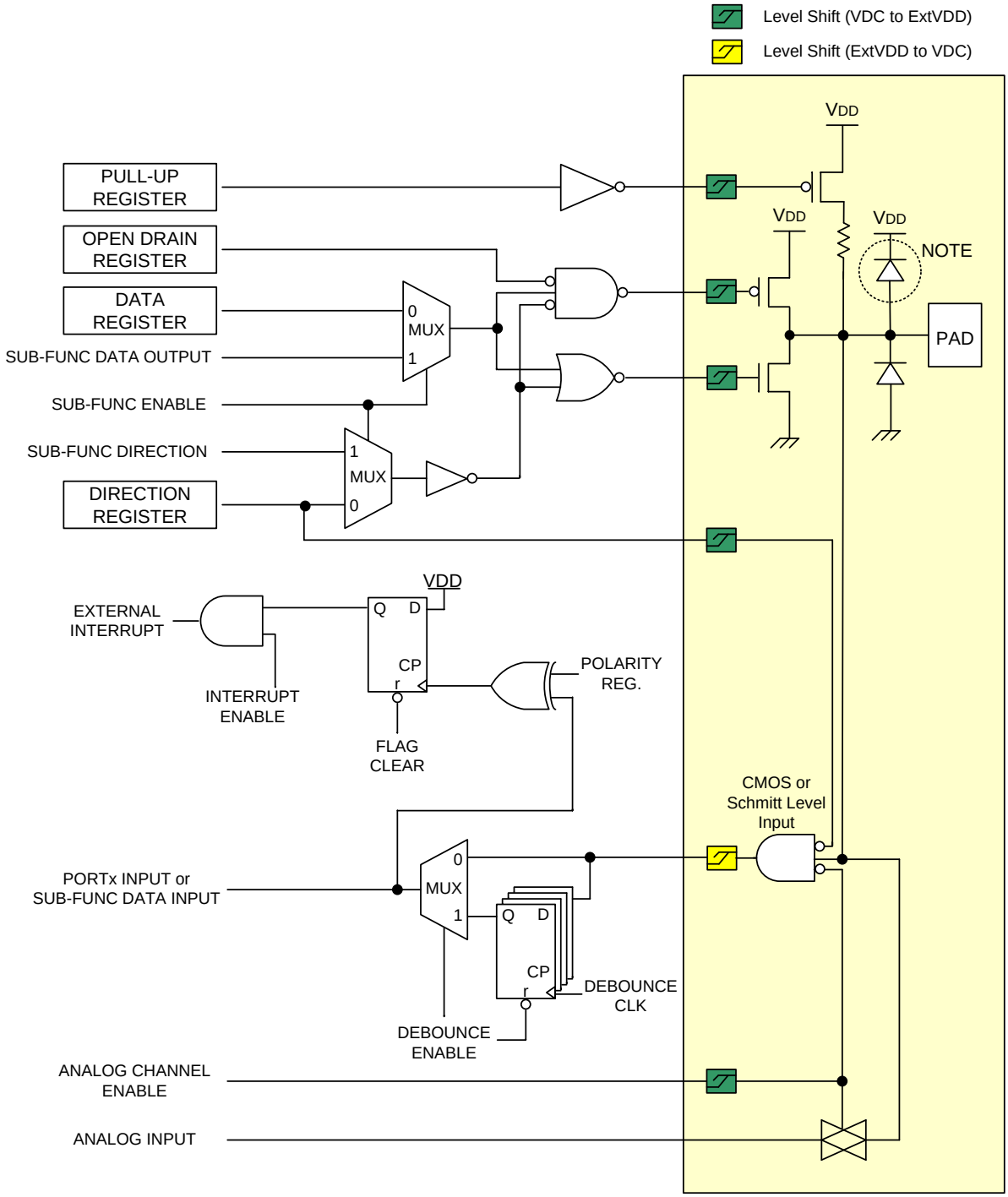
6.1 General Purpose I/O Port



NOTE)
The P0, P1, P2, P3, and P5 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port



NOTE)

1. The P0, P1, P2, P3, and P5 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +4.0	V	–
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to Vss
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-80	mA	Maximum current (ΣI_{OH})
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
REM Output Pin	I_{OL}	800	mA	Maximum current sunk by REM pin
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 – +150	℃	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions			Min	Max	Units
Operating Voltage	V_{DD}	fx = 32 – 38kHz	SX-tal		1.8	3.6	V
		fx = 0.4 – 4.2MHz	X-tal,	Ceramic	1.8	3.6	
				Crystal	2.0	3.6	
		fx = 0.4 – 8MHz	X-tal		2.4	3.6	
		fx = 0.4 – 12MHz			3.0	3.6	
		fx = 0.5 – 8MHz	HFIRC		1.8	3.6	
		fx = 4.0 – 32kHz	LFIRC		1.8	3.6	
Operating Temperature	TOPR	VDD = 1.8 – 3.6V			-40	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	10	–	bit
Integral Non-Linear	INL	VDD=2.4V – 3.6V, fx=8MHz		–	–	±3	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	VDD=2.4V – 3.6V		30	–	–	us
		VDD=2.7V – 3.6V		20	–	–	
Analog Input Voltage	V_{AIN}	–		VSS	–	VDD	V
Band Gap Reference Value(4)	VAL_{BGR}	VDD=3.3V, TA=25℃, MSB align, 8 times average, Different from CNFMRR0/1 values and ADC result (“CNFMRR0/1” – “ADC result”)		–	–	±15	LSB
A/DC Input Leakage Current	I_{AIN}	VDD=3.072V		–	–	10	uA
A/DC Current	I_{ADC}	Enable	VDD=3.072V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 0x000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 0x3ff and the converted output for top input voltage (VDD).
3. If VDD is less than 2.4V, the resolution degrades by 1-bit whenever VDD drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)
4. The CNFMRR0/1 register of XRAM has an AD/C result value which reads VBGR voltage at VDD=3.3V. The CNFMRR0 has the value of ADCDRL[7:0] and CNFMRR1 has the value of ADCDRH[7:0].

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.2	–	V
VDD Voltage Rising Time	t_R	0.5V – 2.0V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.4 Power-on Reset Characteristics

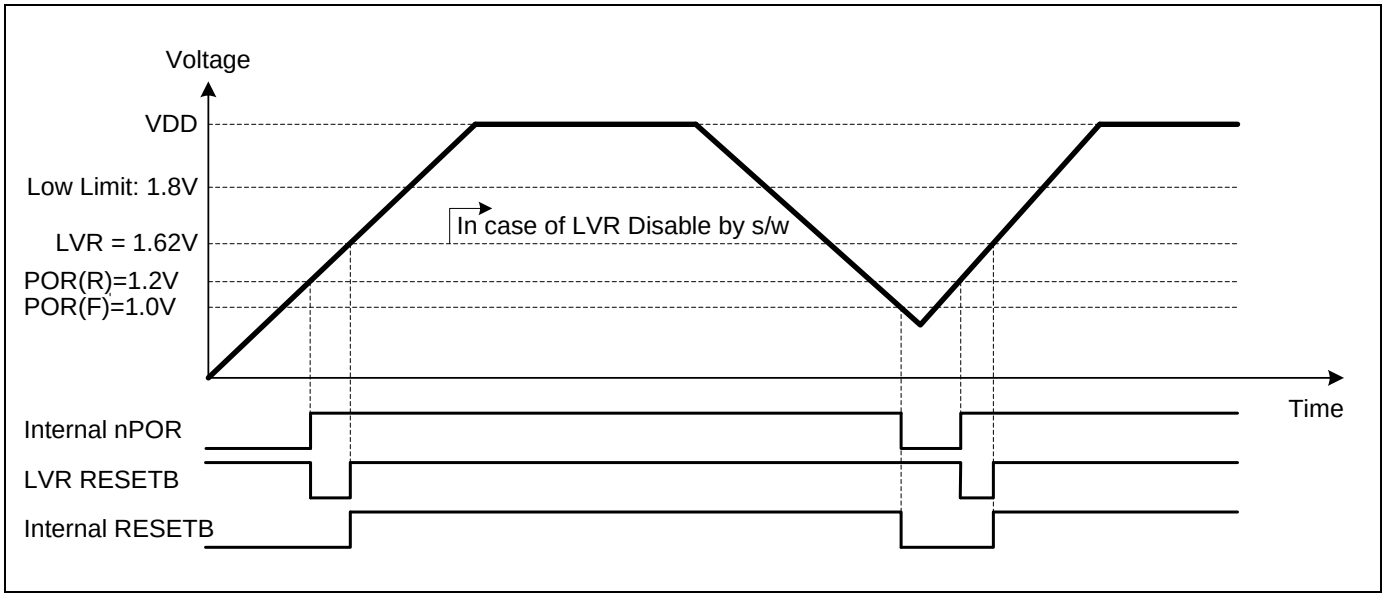


Figure 7.1 Power-on Reset Timing

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.62V.		–	1.62	1.79	V
				1.85	2.00	2.15	
				2.25	2.40	2.55	
				2.53	2.68	2.83	
Hysteresis	△V	–		–	10	50	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD=3V, Run mode	–	5.0	10.0	uA
		Enable (One of two)		–	4.0	8.0	
		Disable (Both)	VDD=3V	–	–	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 High Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{HFIRC}	VDD = 1.8V – 3.6V		–	8	–	MHz
Tolerance	–	T_A = -10 °C to +55°C	With 0.1uF bypass capacitor	-2.0	–	+2.0	%
		T_A = -20 °C to +85°C		-3.0	–	+3.0	
		T_A = -40 °C to +85°C		-4.0	–	+4.0	
		T_A = -10 °C to +55°C (User trim, Using E-PGM+ or S/W)		-1.0	–	+1.0	
Clock duty ratio	TOD	–		40	50	60	%
Stabilization Time	t_{HFS}	–		–	–	100	us
HFIRC Current	I_{HFIRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.6 High Frequency Internal RC Oscillator Characteristics

NOTE)

1. User Trimming means the calibration of HFIRC frequency. Using E-PGM +.
2. To ensure ±1.0% tolerance of HFIRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design, but might be On-Board programming after SMT process.
   (HFIRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate Enough to cool to near room temperature after SMT process)

7.7 Low Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{LFIRC}	VDD = 1.8V – 3.6V		–	32	–	kHz
Tolerance	–	T_A = -10 °C to + 55°C	With 0.1uF bypass capacitor	-10.0	–	+10.0	%
Clock duty ratio	TOD	–		40	50	60	%
Stabilization Time	t_{LFS}	–		–	–	1	ms
LFIRC Current	I_{LFIRC}	Enable	VDD=3.0V	–	2	–	uA
		Disable		–	–	0.1	

Table 7.7 Low Frequency Internal RC Oscillator Characteristics

7.8 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.8 Internal WDTRC Oscillator Characteristics

7.9 LCD Voltage Characteristics

(T_A= -40°C ~ +85°C, VDD=2.0V ~ 3.6V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LCD Voltage	V_{LC3}	Voltage booster enabled, 1/2 bias	Typx0.93	1.0+(Nx0.05)	Typx1.07	V
		Voltage booster enabled, 1/3 bias	Typx0.93	0.75	Typx1.07	
				0.79		
				0.83		
				0.86		
				0.90		
				0.94		
				0.98		
				1.01		
				1.05		
				1.09		
LCD Mid Bias Voltage	$V_{LC0/2}$	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1	V
	V_{LC0}	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V	Typx0.9	3xVLC3	Typx1.1	
	V_{LC2}		Typx0.9	2xVLC3	Typx1.1	
	V_{LC2}	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 3.6V, 1/3 bias, LCD clock = 0Hz, VLC0=VDD	Typ-0.2	0.67xVDD	Typ+0.2	V
	V_{LC3}		Typ-0.2	0.33xVDD	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	V_{LCD}=3V, I_{LOAD}=±10uA	–	5	10	kΩ
LCD Bias Dividing Resistor	R_{LCD1}	Internal resistor mode, T_A = 25°C	20	30	40	kΩ
	R_{LCD2}		40	60	80	
	R_{LCD3}		80	120	160	
LCD Block Current	I_{LCD}	Voltage booster mode, VDD=3V, V_{LCD}=3.15V, 1/3Bias	–	3	6	uA

Table 7.9 LCD Voltage Characteristics

NOTE)

1. Where N is the value of LCDCCR register (N = 0 to 9).

7.10 DC Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	V_{IH1}	P17, P20, P3, P4, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except VIH1		0.7VDD	–	VDD	
Input Low Voltage	V_{IL1}	P17, P20 P3, P4, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except VIL1		–	–	0.3VDD	
Output High Voltage	V_{OH}	VDD=3.3V, IOH = – 2mA; All output ports except REM pin		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=3.3V, IOL=10mA; All output ports except VOL2 and REM		–	–	1.0	V
	V_{OL2}	VDD=3.0V, LCDBL0 and LCDBL1	IOL=10mA, DRV = 0	–	–	1.0	V
			IOL=20mA, DRV = 1				
			IOL=30mA, DRV = 2				
Inverter Amp Output Current	I_{OHA}	VDD=3V, VOH=2.5V VO0, VO1, and VO2	TA=25°C	-700	-400	-200	uA
	I_{OLA}	VDD=3V, VOL=0.5V VO0, VO1, and VO2		200	400	700	
REM Output High Current	I_{OHR}	VDD=3.0V, VOH=2.0V, ROTS=1		–	-10	-5	mA
REM Output Low Current	I_{OL1}	VDD=3.0V, V_{OL}=1.0V, TA=25°C	ROTS=1	2.5	5.0	–	mA
	I_{OL2}		ROTS=0, RIOL=3	470	630	–	
Input high leakage current	I_{IH}	All Input ports		–	–	1	uA
Input low leakage current	I_{IL}	All Input ports		-1	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=3V	50	100	200	kΩ
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=3V	200	400	800	
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS TA=25°C, VDD=3V FBS = 0 (Configure Option 2: 1FH)		1200	2400	3500	kΩ
		XIN=VDD, XOUT=VSS TA=25°C, VDD=3V FBS = 1 (Configure Option 2: 1FH)		500	1000	1500	
	R_{X2}	SXIN=VDD, SXOUT=VSS TA=25°C, VDD=3V		5	10	20	MΩ

Table 7.10 DC Characteristics

7.11 DC Characteristics (Continued)

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current	I_{DD1} (Run)	f_{XIN}=12MHz, VDD=3V±10%		–	1.5	3.0	mA
		f_{HFIRC}=8MHz, VDD=3V±10%		–	1.0	2.0	
		f_{XIN}=8MHz, VDD=3V±10%		–	1.0	2.0	
	I_{DD2} (Idle)	f_{XIN}=12MHz, VDD=3V±10%		–	0.5	1.0	mA
		f_{HFIRC}=8MHz, VDD=3V±10%		–	0.4	0.8	
		f_{XIN}=8MHz, VDD=3V±10%		–	0.4	0.8	
	I_{DD3} (Run)	f_{SUB}=32.768kHz	VDD=3V±10%, TA=25°C	–	70	140	uA
		f_{LFIRC}=32kHz		–	70	140	
	I_{DD4} (Idle)	f_{SUB}=32.768kHz		–	4.0	8.0	uA
		f_{LFIRC}=32kHz		–	4.0	8.0	
	I_{DD5}	Stop, VDD=3V±10%, TA=25°C		–	0.5	3.0	uA

Table 7.11 DC Characteristics (Continued)

NOTE)

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator, the f_{HFIRC} is an internal high frequency RC oscillator, the f_{LFIRC} is an internal low frequency RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.11 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 3.6V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 3 V	10	–	–	us
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 3 V	200	–	–	ns
REM port High, Low width	t_{REMWH}, t_{REMWL}	REM, VDD = 3 V	5	–	–	us

Table 7.11 AC Characteristics

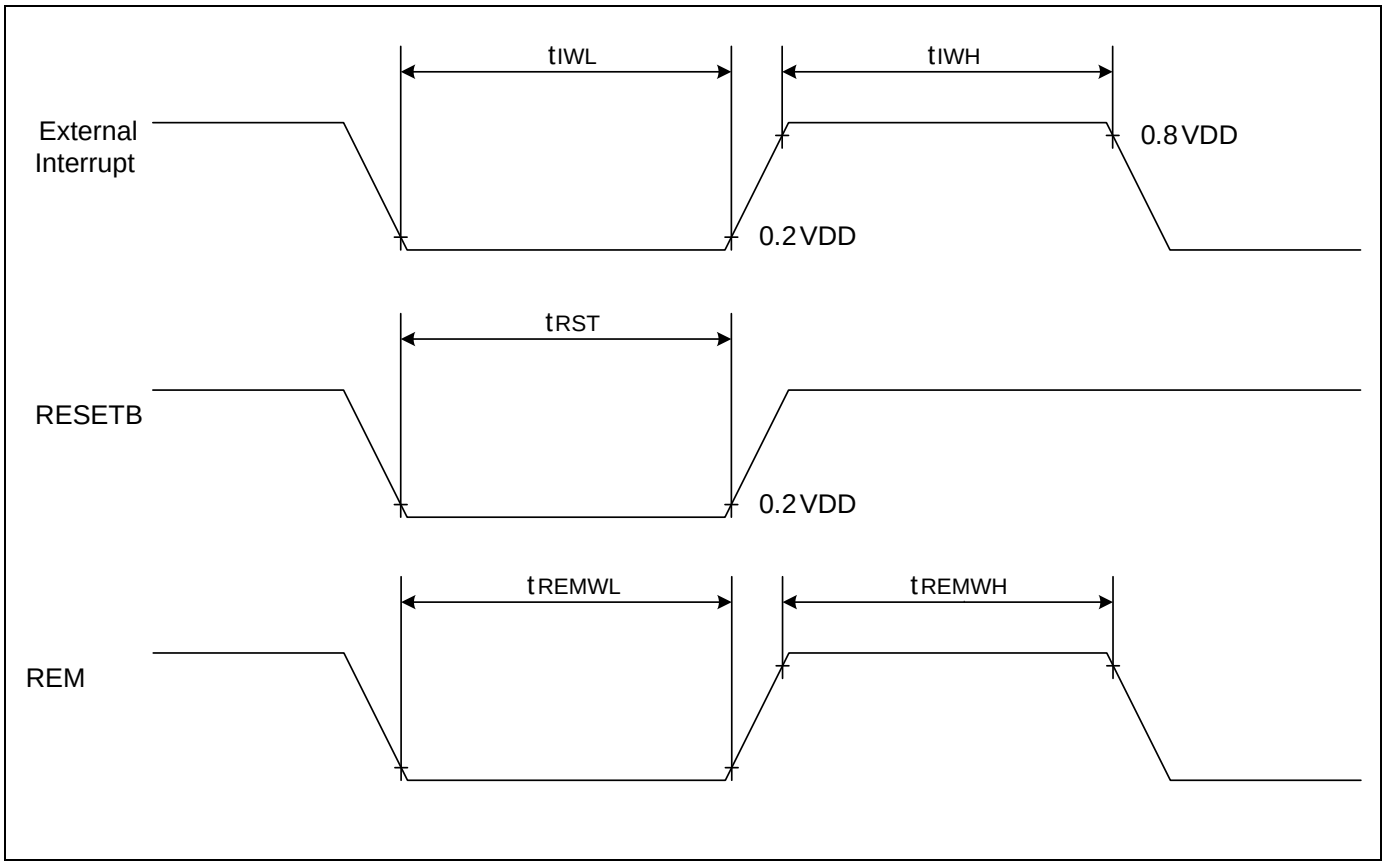


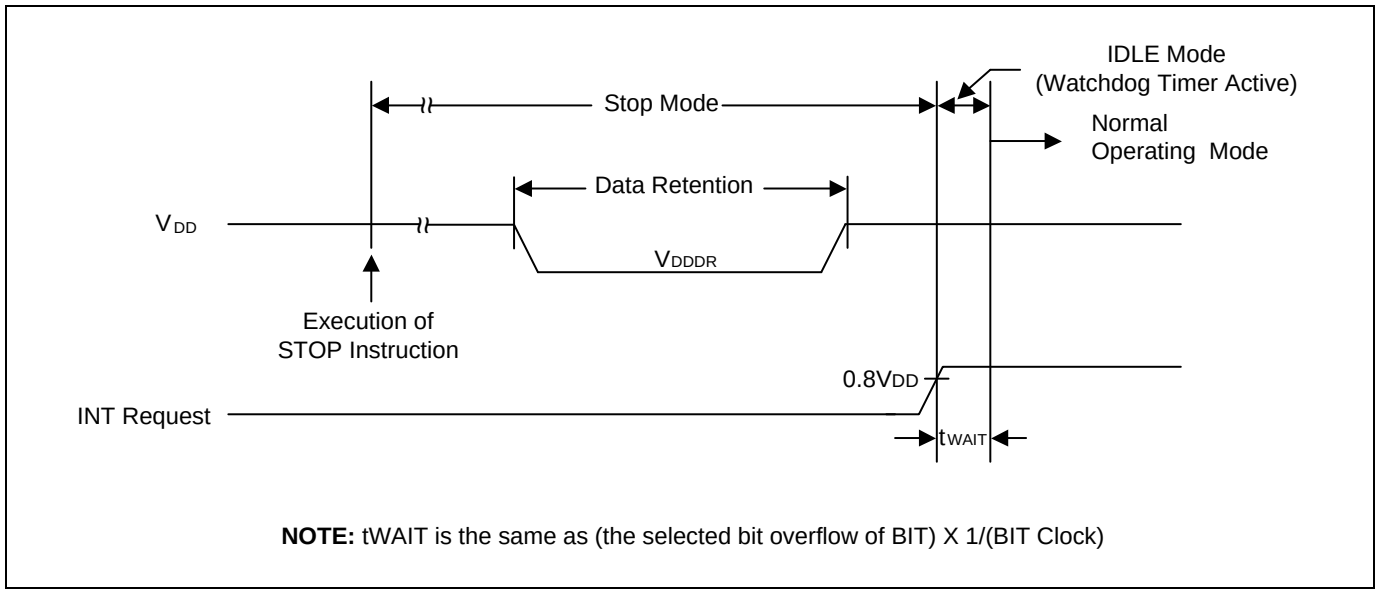
Figure 7.2 AC Timing

7.12 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V)

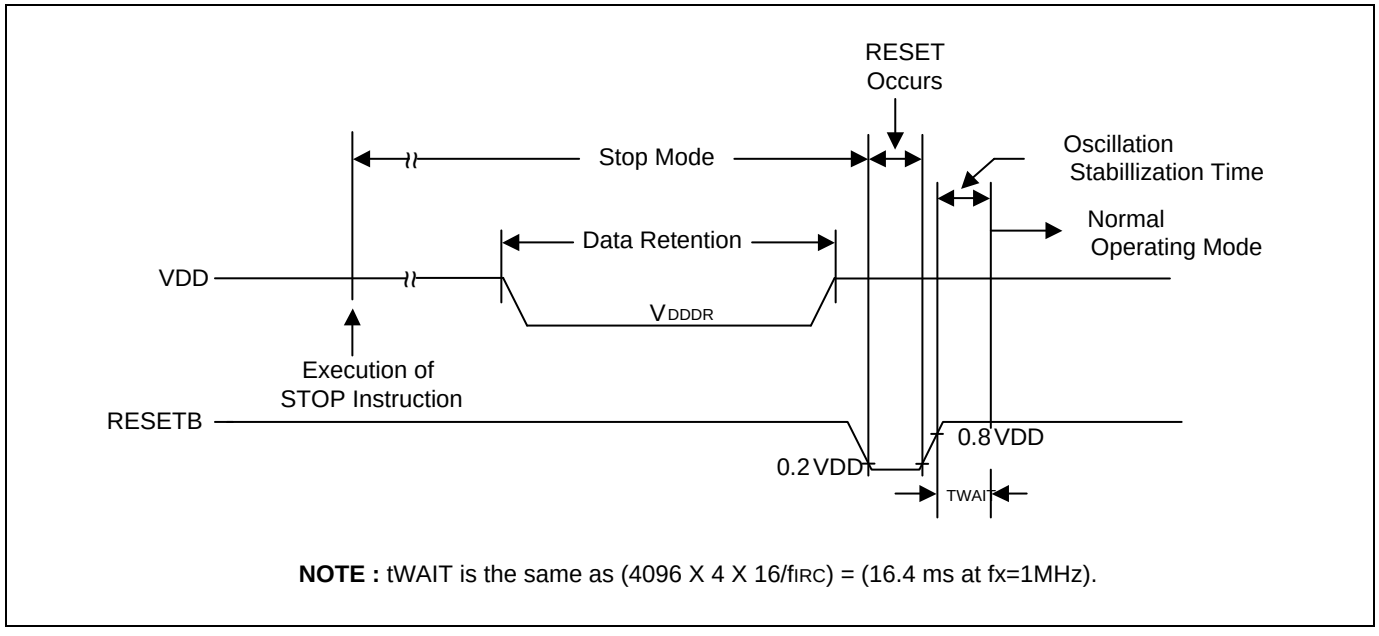
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.0	–	3.6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V (T_A = 25°C), Stop mode	–	–	1	uA

Table 7.12 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.3 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (16.4 ms at fx=1MHz).

Figure 7.4 Stop Mode Release Timing when Initiated by RESETB

7.13 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	3.0	3.2	
Hard-Lock Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	Sector 0 to 375	–	–	10,000	Times
		Sector 376 to 383	–	–	100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Table 7.13 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (HF INT-RC OSC or Main X-TAL for system clock).

7.14 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{IN}	fx=1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.14 Input/Output Capacitance

7.15 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Main oscillation frequency	2.0 V – 3.6 V	0.4	–	4.2	MHz
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8 V – 3.6 V	0.4	–	4.2	
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	
External Clock	XIN input frequency	1.8 V – 3.6 V	0.4	–	4.2	MHz
		2.4 V – 3.6 V	0.4	–	8.0	
		3.0 V – 3.6 V	0.4	–	12.0	

Table 7.15 Main Clock Oscillator Characteristics

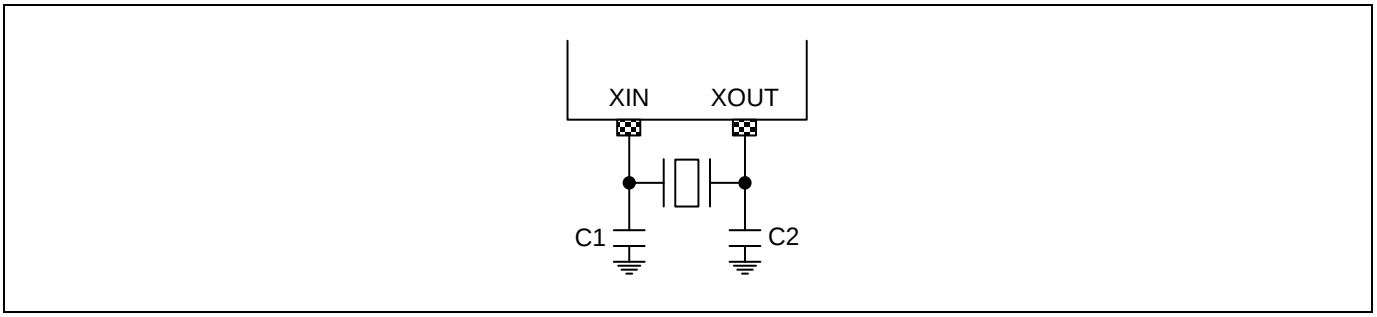


Figure 7.5 Crystal/Ceramic Oscillator

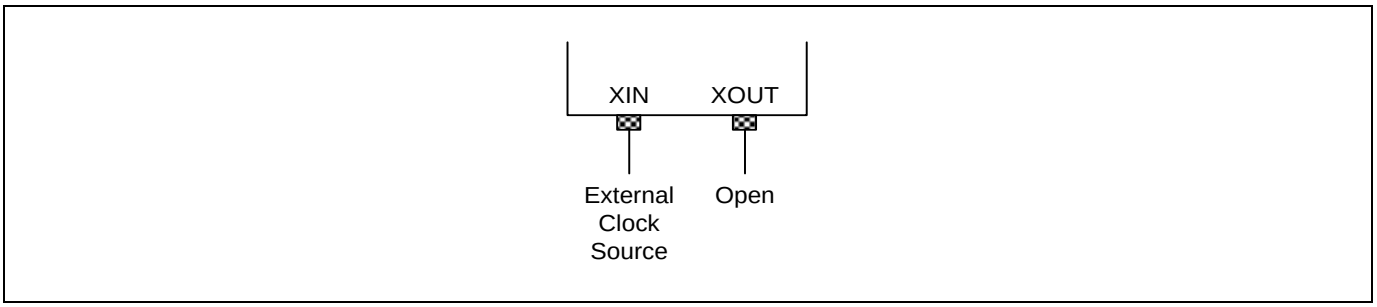


Figure 7.6 External Clock

7.16 Sub Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 3.6V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 3.6 V	32	32.768	38	kHz

Table 7.16 Sub Clock Oscillator Characteristics

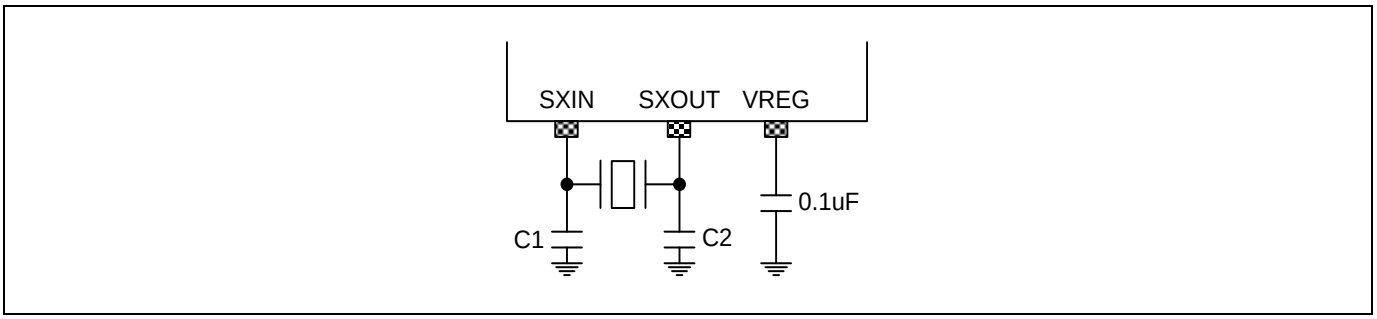


Figure 7.7 Crystal Oscillator

7.17 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 3.6V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	fXIN ≥ 1 MHz, VDD = 2.0V~3.6V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic	fXIN ≥ 1 MHz, VDD = 1.8V~3.6V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	10	
External Clock	fXIN = 0.4 to 12 MHz XIN input high and low width (tXL, tXH)	42	–	1250	ns

Table 7.17 Main Oscillation Stabilization Characteristics

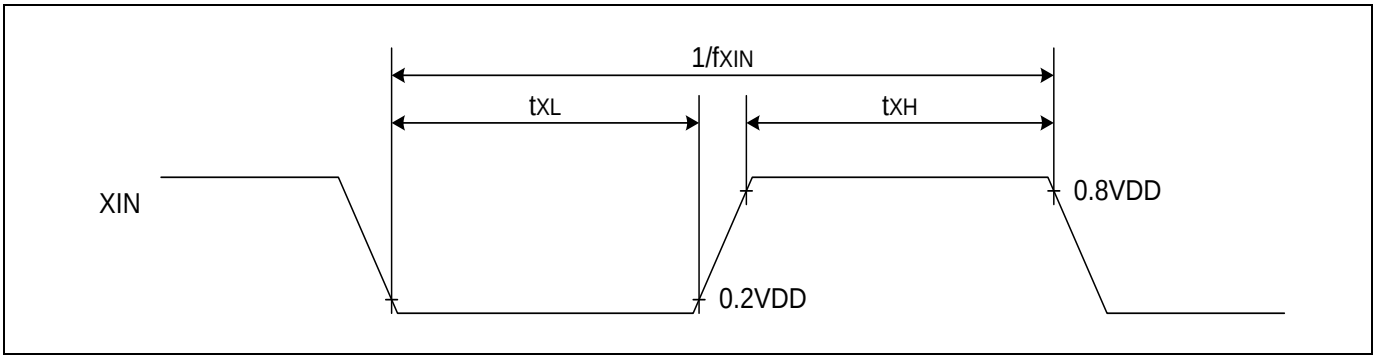


Figure 7.8 Clock Timing Measurement at XIN

7.18 Sub Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 3.6V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD = 3.0V, T_A = 25°C	–	0.7	1.5	
External Clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	us

Table 7.18 Sub Oscillation Stabilization Characteristics

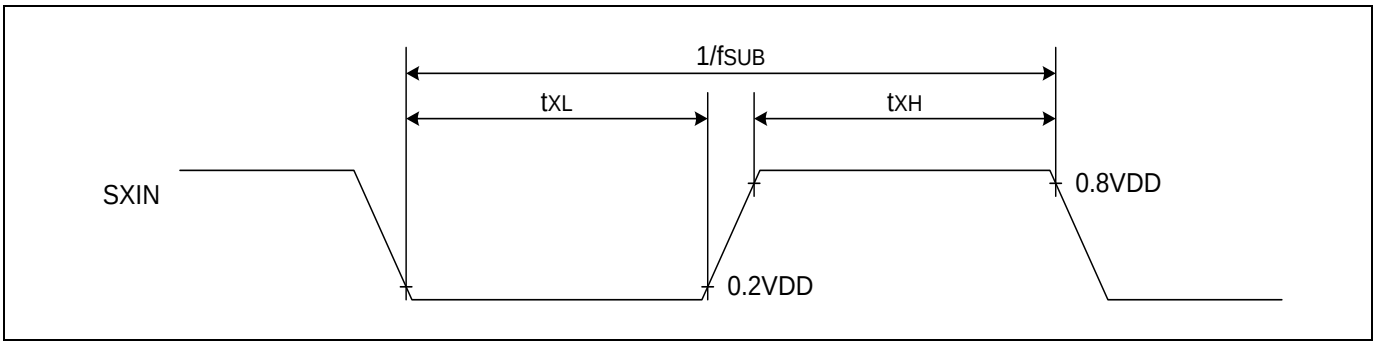


Figure 7.9 Clock Timing Measurement at SXIN

7.19 Operating Voltage Range

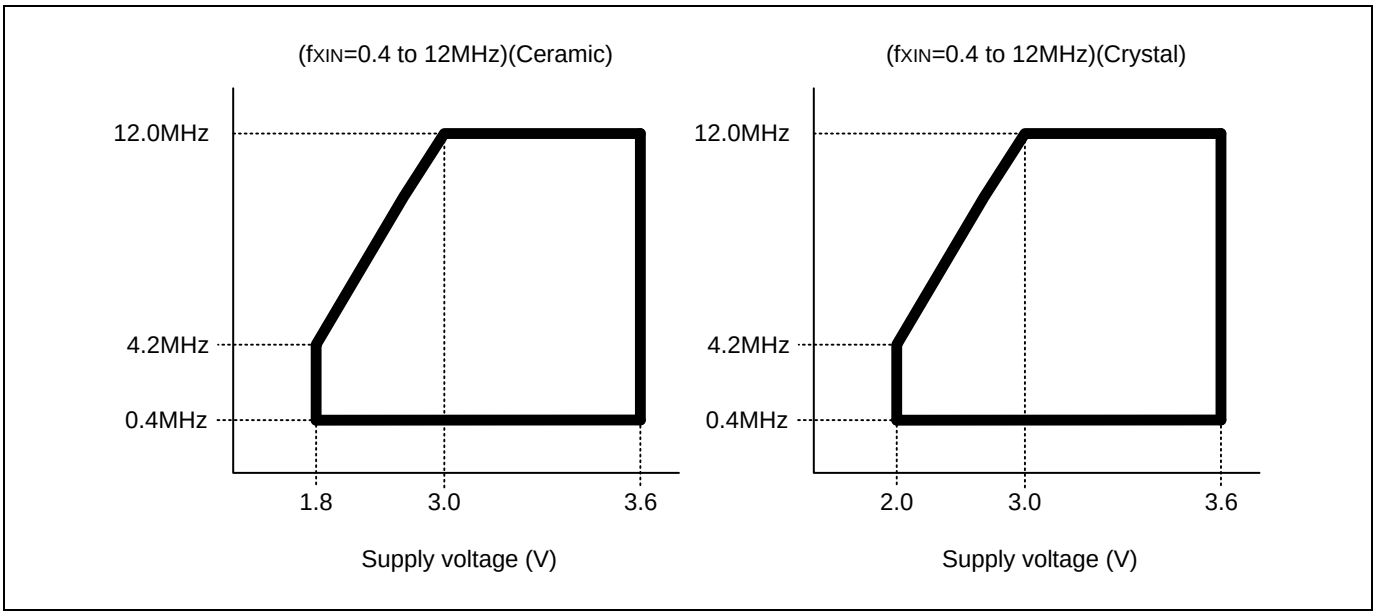


Figure 7.10 Operating Voltage Range (Main OSC)

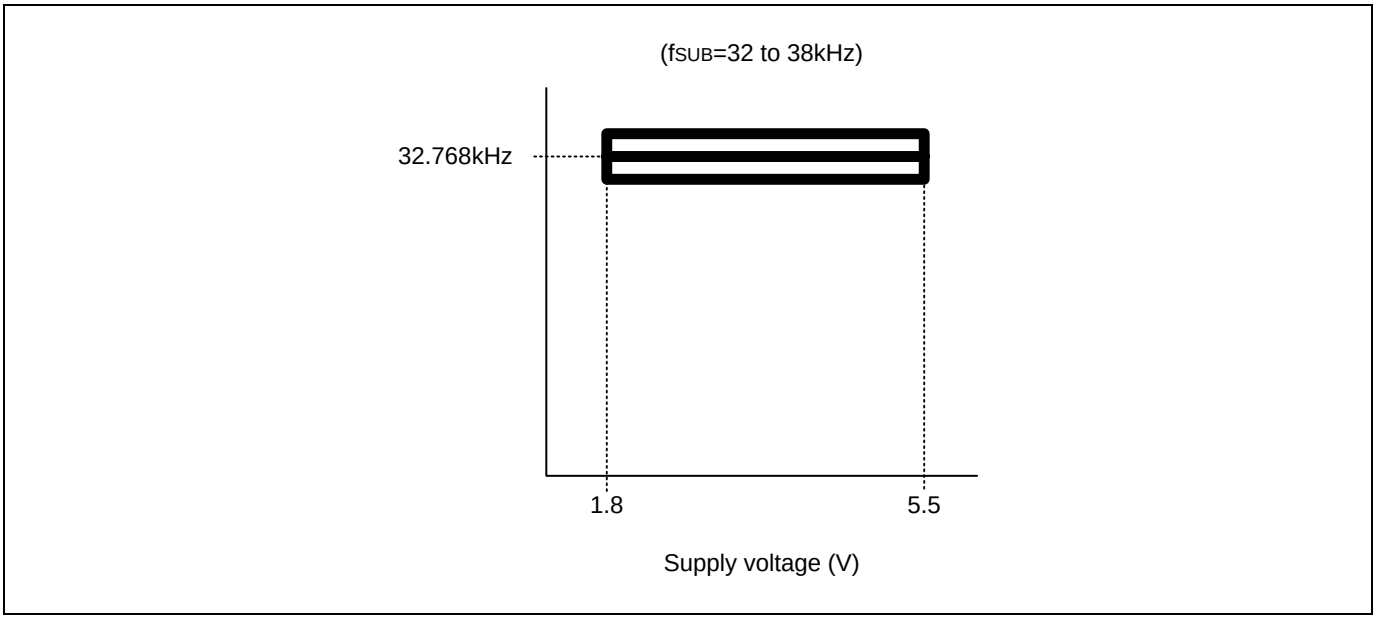


Figure 7.11 Operating Voltage Range (Sub OSC)

7.20 Recommended Circuit and Layout

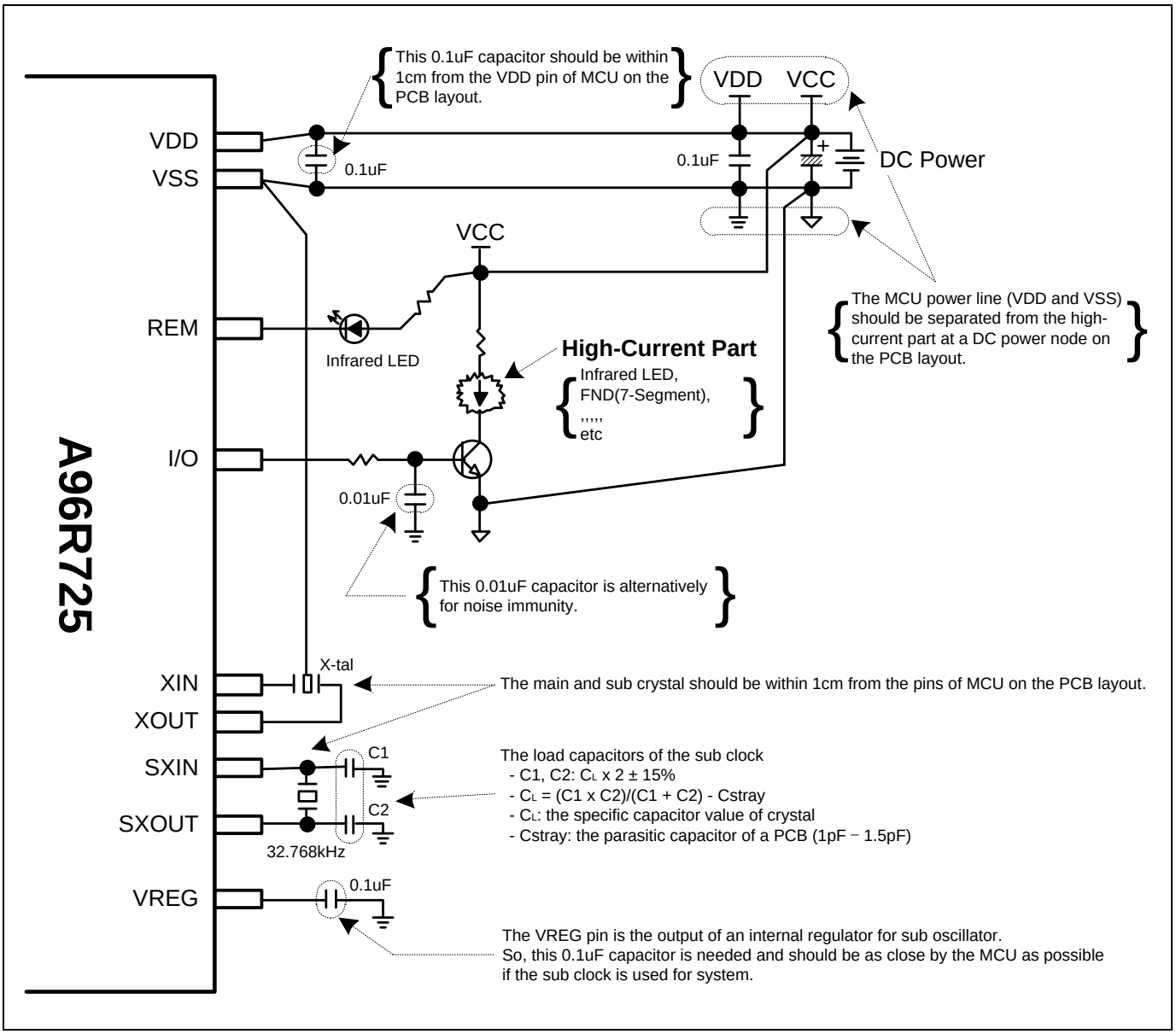


Figure 7.12 Recommended Circuit and Layout

7.21 Recommended Circuit for Remote controller

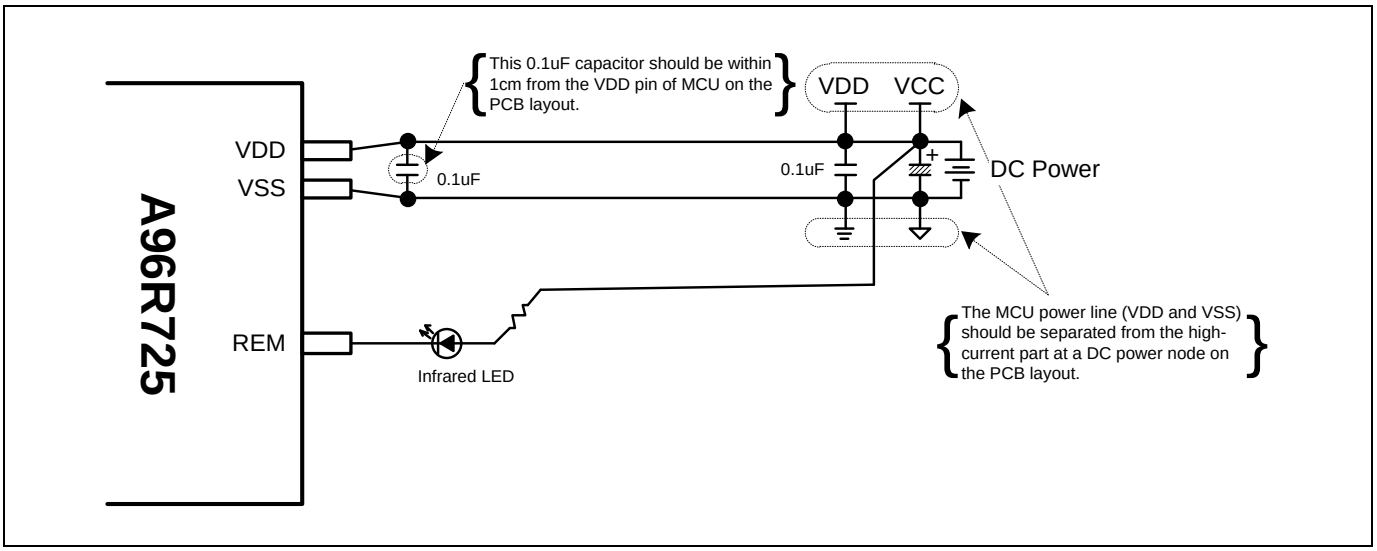
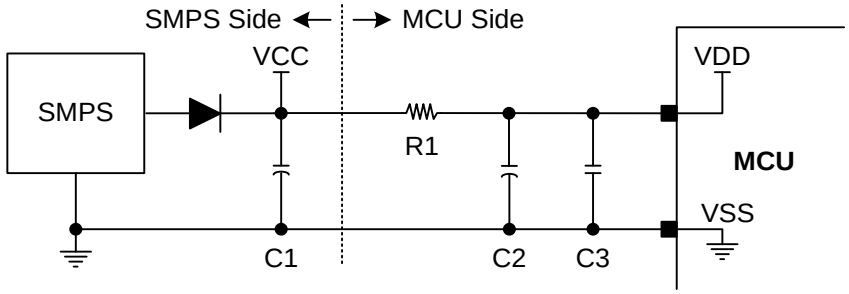


Figure 7.13 Recommended Circuit for Remote controller

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.14 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

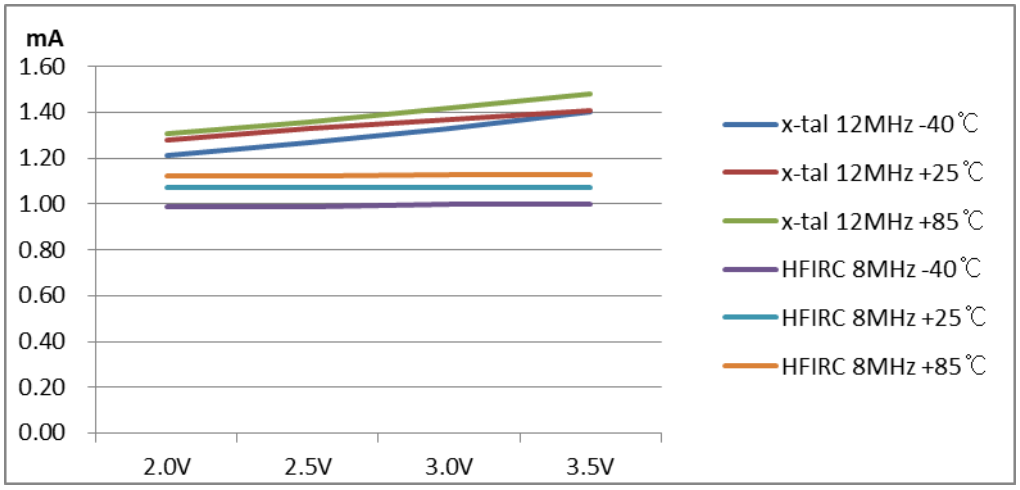


Figure 7.15 RUN (IDD1) Current

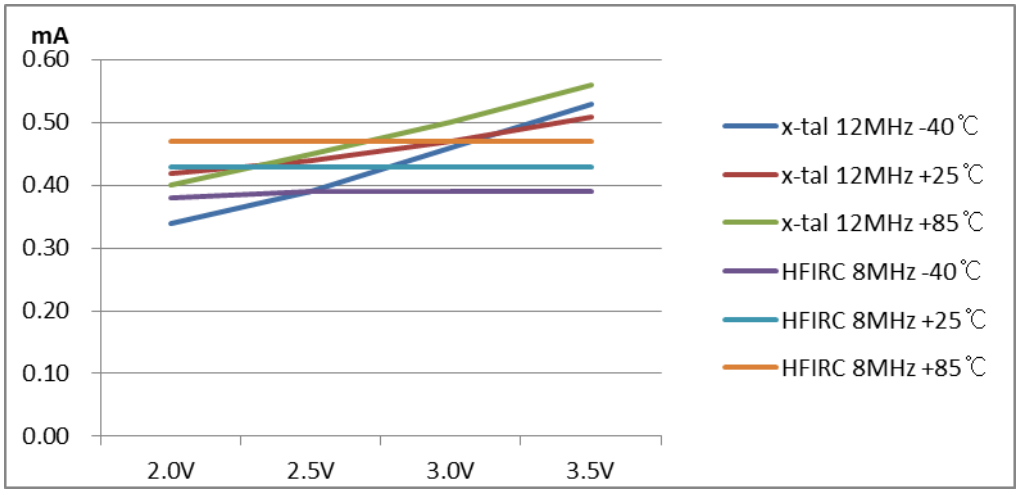


Figure 7.16 IDLE (IDD2) Current

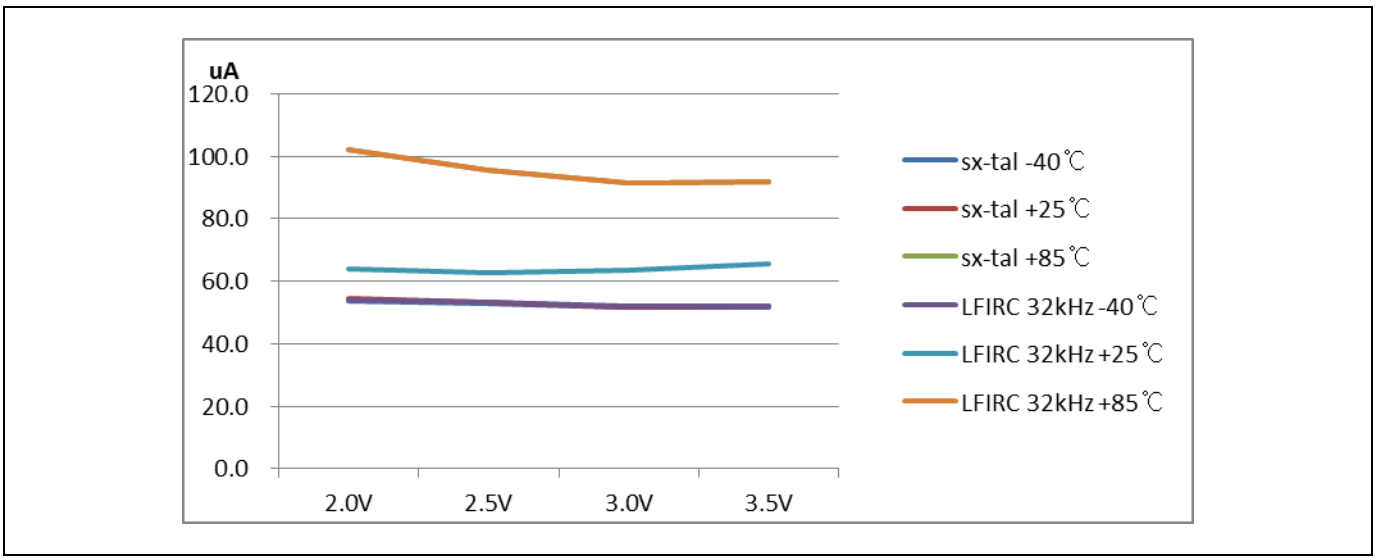


Figure 7.17 RUN (IDD3) Current

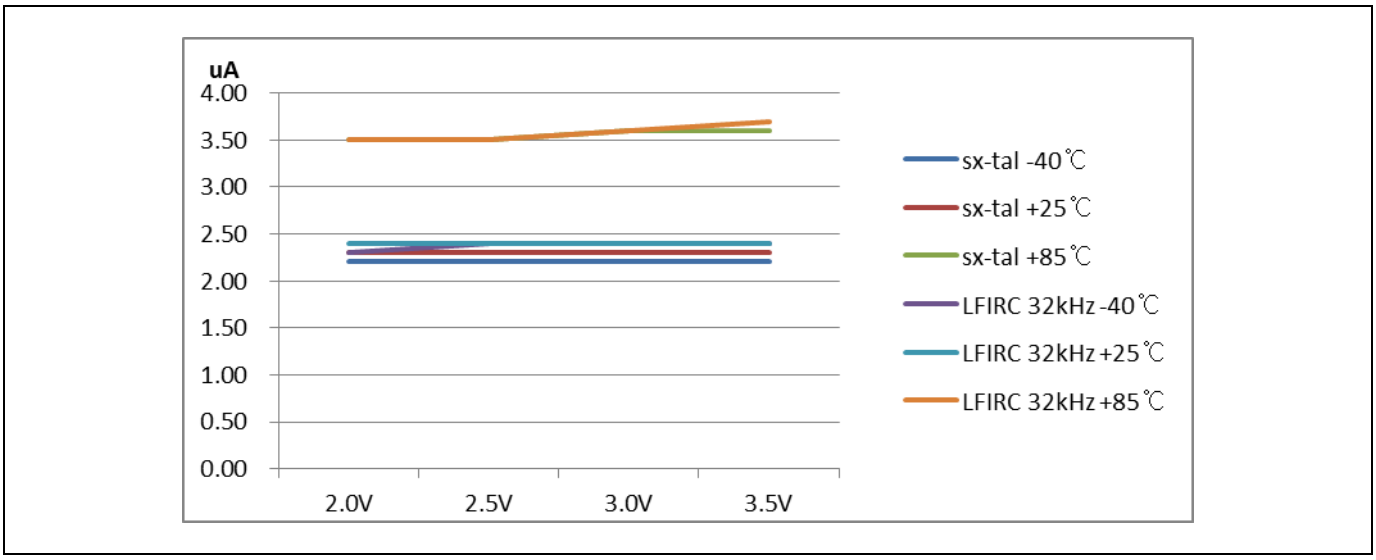


Figure 7.18 IDLE (IDD4) Current

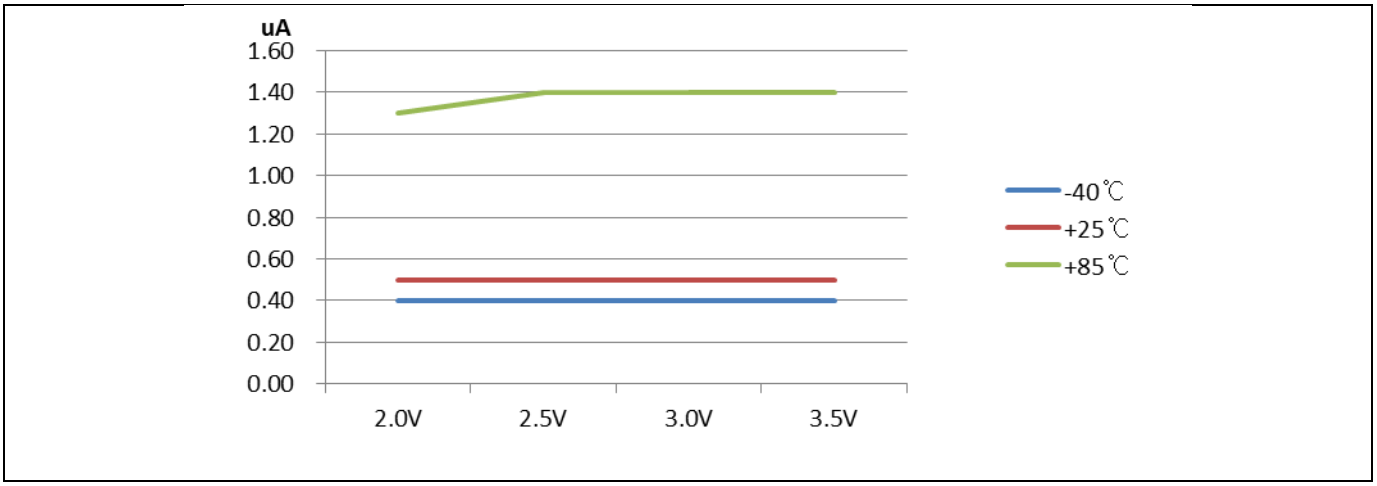


Figure 7.19 STOP (IDD5) Current

Table of contents