16 Channel Constant Currnet LED Sink Driver

Features

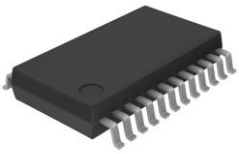
- Supply Voltage Range: 4.5~5.5V
- 16 channel constant sink current output
- Constant output current range: 3~60mA
- Constant current output voltage: 17V(max.)
- Current Accuracy
  - Between channels :3%(typ.)
  - Between ICs : 6%(typ.)
- Fast response of output current
- Min. output pulse width of OEB : 200ns

Descriptions

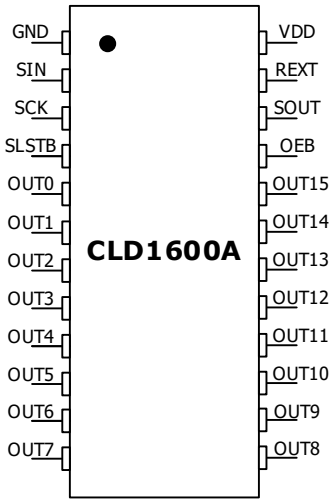
The CLD1600A is a 16-channel constant current sink driver for LEDs. The CLD1600A is comprised of a 16-bit shift-register, a 16-bit output latch and 16 output drivers, which is designed for serial input and parallel output format. The 16 regulated output currents are adjusted through an external resister.

Package Info.

- 24-LEAD SSOP



Pin Configuration



Terminal Description

Name	I/O	PIN	Description
GND	P	1	The ground pin
SIN	I	2	The serial data input
SCK	I	3	The serial data transfer clock input pin
SLATB	I	4	The latch signal input pin. Data is saved at Low Level.
OUTn	O	5~20	A sink type constant current output pin
OEB	I	21	Enable the output current. Output is off at High Level.
SOUT	O	22	The serial data output pin
REXT	B	23	The current value setting pin
VDD	P	24	The power supply

Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted

Symbol	Rating	Max	Unit
VDD	Supply Voltage	7	V
IP/IM	Input Voltage	-0.3 to VDD+0.3	V
T_A	Operating free-air temperature range	-40 to 85	°C
T_J	Operating junction temperature range	-40 to 150	°C
Tstg	Storage temperature range	-55 to 150	°C
	ESD Protection Human Body Model (HBM) (Note 1) Machine Model (MM) (Note2) Charged Device Model(CDM)	 TBD TBD TBD	V

Stresses exceeding those listed under absolute maximum ratings may cause permanent damage to device.

1. Human Body Model: 100pF discharged through a 1.5k resistor following specification JESD22/A114.
2. Machine Model: 200pF discharged through all pins following specification JESD22/A115.

Recommended Operating Conditions

Symbol	Rating	MIN	MAX	Unit
VDD	Supply Voltage	4.5	5.5	V
VIH	High-level input Voltage (SIN,SCK,SLATB,OEB)	0.7*VDD	VDD	V
VIL	Low-level input Voltage (SIN,SCK,SLATB,OEB)	0	0.3*VDD	V
T_A	Operating free-air temperature range	-40	85	°C

Operating Characteristics

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Power supply voltage		V_{DD}		4.5		5.5	V
Output terminal voltage		V_{OUT}	OUT0~OUT15			17	V
Output current		I_{OUT}	OUT0~OUT15, DC	3		60	mA
		I_{OH}	SOUT			-1	mA
		I_{OL}	SOUT			1	mA
Input voltage	'H'	V_{IH}		0.7VDD		VDD	V
	'L'	V_{IL}		GND		0.3VDD	V
Output voltage	'H'	V_{OH}	SOUT	0.9VDD		VDD	V
	'L'	V_{OL}	SOUT	GND		0.1VDD	V
Current error		D_{IOUT1}	CH to CH		±3		%
			Chip to Chip		±6		%
Constant current vs. output voltage regulation		D_{IOUT2}	VOUT within 1V to 3V		±0.1		%/V
Constant current vs. supply voltage regulation		D_{IOUT3}	VDD within 4.5V to 5.5V		±0.1		%/V
Pull up resistor		R_{UP}		120	200		kΩ
Pull down resistor		R_{DOWN}		120	200		kΩ
Supply current	OFF	I_{DD}(OFF)			7		mA
	ON	I_{DD}(ON)	IOUT=60 mA		14		mA

Switching Characteristics

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Propagation delay	CLK-OUTn	t_{pLH1}	V_{DD}=5 V V_{OUT}=0.8 V V_{IH}=VDD V_{IL}=GND I_{OUT}=60 mA V_L=4 V* R_L=52 Ω** C_L=10 pF**		50		ns
	SLATB-OUTn	t_{pLH2}			50		ns
	OEB-OUTn	t_{pLH3}			20		ns
	CLK-SOUT	t_{pLH}			20		ns
Propagation delay	CLK-OUTn	t_{pHL1}			100		ns
	SLATB-OUTn	t_{pHL2}			100		ns
	OEB-OUTn	t_{pHL3}			50		ns
	CLK-SOUT	t_{pHL}			20		ns
Pulse width	CLK	$t_{W(CLK)}$		20			ns
	SLATB	$t_{W(L)}$		20			ns
	OEB	$t_{W(OEB)}$		200			ns
Hold time for SLATB		$t_{H(L)}$			TBD		ns
Setup time		$t_{su(L)}$			TBD		ns
Hold time for SIN		$t_{H(D)}$			TBD		ns
Setup time for SIN		$t_{su(D)}$			TBD		
Clock frequency		f_{CLK}	Cascade operation		25		MHz
CLK rise time		t_r			TBD		ns
CLK fall time		t_f			TBD		ns

Note. 1 VL means the load supply voltage

2. RL and CL mean the resistor and capacitor in parallel between load supply and OUTn